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EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,560	BOGGS ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *9-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *November 15, 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *appendix "A"*.

DETAILED ACTION

Continuation-in-Part

1. This application is a continuation-in-part of application No. 10/337,949, filed on January 7, 2003. The examiner has reviewed the prior art used in the parent application. MPEP 2001.06(b).

Election / Restriction

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9 and 19-23, drawn to an electronic substrate for interconnecting electronic components, classified in class 174, subclass 260.

II. Claims 10-18, drawn to a method of making a substrate for interconnecting electronic components, classified in class 29, subclass 852.

The inventions are distinct, each from the other because of the following reasons:

3. Inventions group I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case product as claimed can be made by another and materially different process, such as the product with cavity can be made by using respective layers with preformed holes and assembling them instead of forming cavity in

a substrate after forming the substrate. Further, a conductive eyelet can be inserted instead of depositing an electrically conductive material to form a liner.

4. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

5. If group I is elected, the claims are further subject to an election of species, for being drawn to more than a single species, defined as follows:

Specie I	Figure 3-4.
Specie II	Figure 5-6.
Specie III	Figure 7-8

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claims 1 and 19 are generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

6. During a telephone conversation with Robert Watt (Reg. 45,890) on January 31, 2005, a provisional election was made without traverse to prosecute the invention of group I, specie III, reading on figure 7-8, claims 1-9 and 19-23. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. Upon further review of the application, claim 9, with limitation "the base having a larger diameter than the opening" is found not reading on the elected specie, figure 7-8. This limitation reads on non-elected species of figure 3-4 and 5-6. Therefore, claim 9 is further withdrawn from considerations.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

8. The abstract of the disclosure is objected to because of the presence of legal phraseology "comprises" in the abstract. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-7 and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Frankeny et al., US Patent No. 5,745,333.

Regarding claim 1, Frankeny et al., in figure 22, discloses an electronic substrate for interconnecting electronic components, comprising: a substrate (41) having one conductive inner layer ("L1", see marked up figure 22 in appendix "A", shown in more detail in figure 7 as element 1); and one interconnect cavity (cavity for via 48, shown in detail in figure 3 as opening 8) extending into the substrate to expose one of the inner layers ("L1").

Regarding claim 2, Frankeny et al., further discloses one electrically conductive surface layer ("L2", see marked up figure 22 in appendix "A", shown in more detail in figure 5 and 7 as element 9,12), wherein one of the interconnect cavities (cavity for via 48) extends from one of the surface layers ("L2") to one of the inner layer ("L1").

Regarding claim 3, Frankeny et al., further discloses each interconnect cavity comprises a base (base of the cavity for via 48, shown in detail in figure 3 as opening 8) adjacent to one of the inner layer ("L1"), the base comprising a layer of electrically conductive material (9,12, shown in detail in figure 5 and 7).

Regarding claim 4, Frankeny et al., further discloses each interconnect cavity comprises a base (base of the cavity for via 48, shown in detail in figure 3 as element 8) adjacent to one of the inner layer ("L1"), wherein each interconnect cavity defines a wall

(wall of the opening 8, figure 3), the interconnect cavity further comprising a conductive material (9,12, shown in detail in figure 5 and 7) forming a liner on the wall and base, the liner interconnected with one inner layer ("L1").

Regarding claim 5, Frankeny et al., further discloses each interconnect cavity comprises a base (base of the cavity for via 48, shown in detail in figure 3 as element 8) adjacent to and electrically interconnected with one of the inner layer ("L1", shown), wherein one interconnect cavity extending from a surface layer ("L2") defines a wall (wall of the opening 8, figure 3), the interconnect cavity further comprising a conductive material (9,12, shown in detail in figure 5 and 7) forming a liner on the wall and base, the liner interconnected with one inner layer ("L1") and the surface layer ("L2").

Regarding claim 6, Frankeny et al., further discloses each interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material (14, shown in more detail in figure 9).

Regarding claim 7, Frankeny et al., further discloses the interconnect cavities are positioned to correspond with land pads of a surface mount technology electrical component (cavity correspond to land pads of electronic component 46).

Regarding claim 19, Frankeny et al., in figure 22, discloses an electronic device comprising: an electronic component (46) having component interconnects (44); and an

electronic substrate (41) for interconnecting electronic components comprising: a substrate (41) having one conductive inner layers ("L1" see marked up figure 22 in appendix "A", shown in more detail in figure 7 as element 1); and one or more interconnect cavity (cavity for via 48, shown in detail in figure 3 as opening 8) extending into a surface of the substrate to expose one inner layer ("L1").

Regarding claim 20, Frankeny et al., further discloses the substrate comprises one electrically conductive surface layer (("L2", see marked up figure 22 in appendix "A", shown in more detail in figure 5 and 7 as element 9,12), wherein one or more of the interconnect cavities (cavity for via 48, shown in detail in figure 3 as opening 8) extends from one of the surface layers (L2) to one of the inner layers (L1).

Regarding claim 21, Frankeny et al., further discloses each interconnect cavity comprises a base (base of the cavity for via 48, shown in detail in figure 3 as opening 8) adjacent to one of the inner layer (L1), the base comprising a layer of electrically conductive material (9,12, shown in detail in figure 5 and 7).

Regarding claim 22, Frankeny et al., further discloses each interconnect cavity comprises a base (base of the cavity for via 48, shown in detail in figure 3 as opening 8) adjacent to one of the inner layer (L1), wherein each interconnect cavity defines a wall (wall of the opening 8, figure 3), the interconnect cavity further comprising a conductive

material (9,12, shown in detail in figure 5 and 7) forming a liner on the wall and base, the liner interconnected with one inner layer (L1).

Regarding claim 23, Frankeny et al., further discloses the electronic component is a microelectronic die (flipchip, see figure 22).

11. Claims 1-8 and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyko et al., US Patent No. 6,660,945.

Regarding claim 1, Boyko et al., in figure 3, discloses an electronic substrate for interconnecting electronic components, comprising: a substrate (100, including substrate 101 and first dielectric layer 118) having one conductive inner layer (112); and one interconnect cavity (119) extending into the substrate to expose one (112) of the inner layers.

Regarding claim 2, Boyko et al., further discloses one electrically conductive surface layer (122), wherein one of the interconnect cavities (119) extends from one of the surface layers to one of the inner layer (122).

Regarding claim 3, Boyko et al., further discloses each interconnect cavity comprises a base (base of the cavity) adjacent to one of the inner layer (112), the base comprising a layer of electrically conductive material (122, column 5, line 25-35).

Regarding claim 4, Boyko et al., further discloses each interconnect cavity comprises a base (base of cavity 119) adjacent to one of the inner layer (112), wherein each interconnect cavity defines a wall (wall of cavity 119, column 5, line 30-35), the interconnect cavity further comprising a conductive material (122, column 5, line 25-35) forming a liner on the wall and base, the liner interconnected with one inner layer (112).

Regarding claim 5, Boyko et al., further discloses each interconnect cavity comprises a base (base of cavity 119) adjacent to and electrically interconnected with one of the inner layer (112), wherein one or more interconnect cavity extending from a surface layer (122) defines a wall (wall of cavity 119, column 5, line 30-35), the interconnect cavity further comprising a conductive material (122) forming a liner on the wall and base, the liner interconnected with one inner layer (112) and the surface layer (122).

Regarding claim 6, Boyko et al., further discloses each interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material (shown in dotted line in figure 3).

Regarding claim 7, Boyko et al., further discloses the interconnect cavities are positioned to correspond with land pads of a surface mount technology electrical component (shown in dotted line in figure 3).

Regarding claim 8, Boyko et al., further discloses each interconnect cavity (119) comprises a base (base of cavity 119) adjacent to one of the inner layer (112) and an opening (opening of cavity 119) at a surface of the substrate (118), the base having a smaller diameter than the opening (see figure 3).

Regarding claim 19, Boyko et al., in figure 3, discloses an electronic device comprising: an electronic component having component interconnects (shown in dotted line but not labeled, column 5, 35-43); and an electronic substrate for interconnecting electronic components comprising: a substrate (100, including substrate 101 and first dielectric layer 118) having one conductive inner layers (112); and one or more interconnect cavities (119) extending into a surface of the substrate to expose one inner layer (112).

Regarding claim 20, Boyko et al., further discloses the substrate comprises one electrically conductive surface layer (122), wherein one or more of the interconnect cavities (119) extends from one of the surface layers to one of the inner layers (112).

Regarding claim 21, Boyko et al., further discloses each interconnect cavity comprises a base (base of cavity 119) adjacent to one of the inner layer (112), the base comprising a layer of electrically conductive material (122).

Regarding claim 22, Boyko et al., further discloses each interconnect cavity comprises a base (base of cavity 119) adjacent to one of the inner layer (112), wherein each interconnect cavity defines a wall (wall of cavity 119, column 5, line 30-35), the interconnect cavity further comprising a conductive material (122) forming a liner on the wall and base, the liner interconnected with one inner layer (112).

Regarding claim 23, Boyko et al., further discloses the electronic component is a microelectronic die (semiconductor chip, column 5, line 35-43).

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1-7 and 19-23 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, 4, 11 and 15 of copending Application No. 10/337,949, hereafter AP949, filed on December 31, 2003, in view of Boyko et al., US Patent No. 6,660,945.

This is a provisional obviousness-type double patenting rejection.

Regarding claim 1, claim 1 of AP949, discloses an electronic substrate for interconnecting electronic components, comprising: a substrate (line 3) having one conductive inner layer (line 3); and one interconnect cavity (line 5). Claim 1 of AP949 further discloses the cavity interconnected to one or more inner layer but fails to explicitly disclose the cavity extending into the substrate to expose one of the inner layers.

Boyko et al. US Patent No. 6,660,945, in figure 3, discloses an interconnect structure with cavity (119) exposing an inner layer (112) to have direct blind via connection to inner layer to have a highly dense and reliable interconnect structure. A person of ordinary skill in the art would have recognized the advantage of the cavity exposing the inner layer to have direct and reliable connection of the outer surface layer with the inner layer resulting in a highly dense interconnect structure. The cavity of Boyko et al., further discloses a conductive layer on the wall and the base of the cavity providing direct connection between outer and inner layers having opening at the surface layer to receive the interconnect of the connecting component.

Therefore, it would have been obvious to a person of ordinary skill in the art to provide the substrate of claim 1 of AP949 with the cavity exposing the inner layer, as taught by Boyko et al., in order to have direct blind via connection of outer conductive layer with inner layer to have a highly dense and reliable interconnect structure.

Regarding claim 2, the modified circuit board of claim 1 of AP949, further discloses all the features of the claimed invention including one electrically conductive surface layer (line 3, of claim 1 of AP949), wherein one of the interconnect cavities (line 5) extends from one of the surface layers to one of the inner layer (as applied to claim 1 above).

Regarding claim 3, the modified circuit board of claim 1 of AP949, discloses all the features of the claimed invention including each interconnect cavity comprises a base (base of the modified cavity as applied to claim 1 above) adjacent to one of the inner layer. But fails to disclose the base comprising a layer of electrically conductive material. Boyko et al., in figure 3, further discloses the cavity having a conductive layer on the base and wall of the cavity in order to have direct conductive connection between the outer layer and inner layers. Further, as applied to claim 1 above, cavity with liner on the wall and base will facilitate a direct blind via connection resulting in a highly dense and reliable interconnect.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the structure of claim 1 of AP949 to provide a layer of electrically conductive material on the base and wall of the cavity, as taught by Boyko et al., in order to have direct blind via connection with inner layer to have a highly dense and reliable interconnect.

Regarding claim 4, the modified circuit board of claim 1 of AP949, discloses all the features of the claimed invention including each interconnect cavity comprises a base adjacent to one of the inner layer, wherein each interconnect cavity defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one inner layer, as applied to claim 1 and 3 above.

Regarding claim 5, the modified circuit board of claim 1 of AP949, further discloses each interconnect cavity comprises a base adjacent to and electrically interconnected with one of the inner layer, wherein one or more interconnect cavity extending from a surface layer defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one inner layer and the surface layer, as applied to claims 1 and 3 above.

Regarding claim 6, claim 3 of the AP949 (in combination with modified claim 1 with Boyko et al.), further discloses all the features of the claimed invention including the each interconnect cavity is adapted to receive and interconnect with electrically conductive interconnect material (line 1-3).

Regarding claim 7, claim 4 of the AP949 (in combination with modified claim 1 and 3 with Boyko et al.), further discloses all the features of the claimed invention

including the interconnect cavities positioned to correspond with land pads of a surface mount technology electrical component (line 1-3).

Regarding claim 19, claim 11 of AP949, discloses an electronic device comprising: an electronic component (line 2) having component interconnects (line 2); and an electronic substrate (line 3) for interconnecting electronic components comprising: a substrate having one conductive inner layers (line 4); and one or more interconnect cavities (line 6). Claim 11 of AP949 further discloses the cavity interconnected to one or more inner layers but fails to explicitly disclose the cavity extending into the substrate to expose one of the inner layers.

Boyko et al. US Patent No. 6,660,945, in figure 3, discloses an interconnect structure with cavity (119) exposing an inner layer (112) to have direct blind via connection to inner layer to have a highly dense and reliable interconnect structure. A person of ordinary skill in the art would have recognized the advantage of the cavity exposing the inner layer to have direct and reliable connection of the outer surface layer with the inner layer resulting in a highly dense interconnect structure. The cavity of Boyko et al., further discloses a conductive layer on the wall and the base of the cavity providing direct connection between outer and inner layers having opening at the surface layer to receive the interconnect of the connecting component.

Therefore, it would have been obvious to a person of ordinary skill in the art to provide the substrate of claim 11 of AP949 with the cavity exposing the inner layer, as

taught by Boyko et al., in order to have direct blind via connection of outer conductive layer with inner layer to have a highly dense and reliable interconnect structure.

Regarding claim 20, the modified structure of claim 11 of AP949, discloses all the features of the claimed invention including the substrate comprises one electrically conductive surface layer (line 4-5), wherein one or more of the interconnect cavities (line 6) extends from one of the surface layers to one of the inner layers (as applied to claim 11 above).

Regarding claim 21, the modified circuit board of claim 11 of AP949, discloses all the features of the claimed invention including each interconnect cavity comprises a base (base of the modified cavity as applied to claim 1 above) adjacent to one of the inner layer. But fails to disclose the base comprising a layer of electrically conductive material. Boyko et al., in figure 3, further discloses the cavity having a conductive layer on the base and wall of the cavity in order to have direct conductive connection between the outer layer and inner layers. Further, as applied to claim 1 above, cavity with liner on the wall and base will facilitate a direct blind via connection resulting in a highly dense and reliable interconnect.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the structure of claim 11 of AP949 to provide a layer of electrically conductive material on the base and wall of the cavity, as

taught by Boyko et al., in order to have direct blind via connection with inner layer to have a highly dense and reliable interconnect.

Regarding claim 22, the modified circuit board of claim 11 of AP949 discloses all the features of the claimed invention including each interconnect cavity comprises a base adjacent to one of the inner layer, wherein each interconnect cavity defines a wall, the interconnect cavity further comprising a conductive material forming a liner on the wall and base, the liner interconnected with one inner layer, as applied to claims 19 and 21 above.

Regarding claim 23, claim 15 of the APA949 (in combination of modified claim 19 with Boyko et al.), further discloses the electronic component is a microelectronic die (line 1-2).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huang et al., US Patent No. 6,495,912, in figure 10, discloses a structure with cavity exposing the inner layer.

Carpenter et al., US Patent No. 6,810,583, in figure 3, discloses a circuit structure with cavity exposing the inner layer.

Burgess, US Patent No. 6,631,558, in figure 26, discloses a circuit board with cavity exposing the inner layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IBPatel

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
March 4, 2005